QUICKSWITCH ${ }^{\circledR}$ PRODUCTS
IDTQS3162233

## HIGH-SPEED CMOS

QUICKSWITCH 32:16 MUX/DEMUX

## FEATURES:

- Enhanced N channel FET with no inherent diode to Vcc
- Zero propagation delay, zero ground bounce
- TTL-compatible input and output levels
- Undershoot clamp diodes on all switch and control pins
- Available in 56-pin SSOP and TSSOP Packages


## APPLICATIONS

- Video, audio, graphics switching, muxing
- Hot-swapping, hot-docking
- Voltage translation (5V to 3.3V)
- Bus funneling


## DESCRIPTION:

The QS3162233 is a 32-bit to 16-bithigh-speed CMOS, TTL-compatible switch which can multiplex or demultiplex data. It can be used for memory interleaving where two memory banks need to be addressed simultaniously. It can also be used as two 16-bit to 8-bit multiplexers or as one 32-bit to 16bit multiplexer. SELn inputs control the dataflow. TESTn inputs control either one or two ports connection. The QS3162233 adds an internal $25 \Omega$ series termination resistor to each switch to reduce reflection noise in high-speed applications.

Mux/Demux devices provide an order of magnitude faster speed than equivalent logic devices.

The QS3162233 is characterized for operation at $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$.

FUNCTIONAL BLOCK DIAGRAM


## PIN CONFIGURATION



## PIN DESCRIPTION

| Pin Names | $\mathrm{I} / \mathrm{O}$ | Description |
| :---: | :---: | :--- |
| nA | $\mathrm{I} / \mathrm{O}$ | Bus A |
| $\mathrm{nB} 1, \mathrm{nB} 2$ | $\mathrm{I} / \mathrm{O}$ | Bus B |
| SEL1, SEL2 | I | Data Select |
| TEST1, TEST 2 I | I | Port Select |

## ABSOLUTE MAXIMUM RATINGS ${ }^{(1)}$

| Symbol | Description |  | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: |
| VTERM ${ }^{(2)}$ | Supply Voltage to Ground |  | -0.5 to +7 | V |
| VTERM ${ }^{(3)}$ | DC Switch Voltage Vs |  | -0.5 to +7 | V |
| VTERM ${ }^{(3)}$ | DC Input Voltage VIN |  | -0.5 to +7 | V |
| VAC | AC Input Voltage (pulse width $\leq 20 \mathrm{~ns}$ ) |  | -3 | V |
| Iout | DC Output Current |  | 120 | mA |
| Pmax | Maximum Power <br> Dissipation ( $\mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C}$ ) | SSOP | . 93 | W |
|  |  | TSSOP | . 77 |  |
| Tsta | Storage Temperature |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

## NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc Terminals.
3. All terminals except Vcc .

## CAPACITANCE

( $\mathrm{T} A=+25^{\circ} \mathrm{C}, \mathrm{f}=\mathbf{1 . 0 \mathrm { MHz } , \mathrm { Vin } = 0 \mathrm { V } , \mathrm { VOUT } = 0 \mathrm { V } \text { ) } ) ~ ( 1 )}$

| Pins |  | Typ. | Max. ${ }^{(1)}$ | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Control Inputs |  | 5 | 5.5 | pF |
| Quickswitch Channels <br> (Switch OFF) | Mux | 8.5 | 10 | pF |
|  | Demux | 6 | 7 | pF |

NOTE:

1. This parameter is guaranteed but not production tested.

## FUNCTION TABLE(1)

$\mathrm{n}=1$ through 8

| SEL1 | TEST1 | nA | Function |
| :---: | :---: | :---: | :--- |
| L | L | nB 1 | nA to nB 1 |
| H | L | nB 2 | nA to $\mathrm{nB}_{2}$ |
| X | H | $\mathrm{nB} 1, \mathrm{nB} 2$ | nA to nB 1 and nB 2 |

$\mathrm{n}=9$ through 16

| SEL2 | TEST2 | $n A$ | Function |
| :---: | :---: | :---: | :--- |
| L | L | nB 1 | nA to nB 1 |
| H | L | nB 2 | nA to $\mathrm{nB}_{2}$ |
| X | H | $\mathrm{nB} 1, \mathrm{nB} 2$ | nA to nB 1 and nB 2 |

NOTE:

1. $\mathrm{H}=\mathrm{HIGH}$ Voltage Level

L = LOW Voltage Level
X = Don't Care

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}, \mathrm{Vcc}=5.0 \mathrm{~V} \pm 10 \%$

| Symbol | Parameter | Test Conditions | Min. | Typ. ${ }^{(1)}$ | Max. | Unit |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| VIH | Input HIGH Voltage | Guaranteed Logic HIGH for Control Pins | 2 | - | - | V |
| VIL | Input LOW Voltage | Guaranteed Logic LOW for Control Pins | - | - | 0.8 | V |
| IIN | Input Leakage Current (Control Inputs) | OV $\leq$ VIN $\leq$ Vcc | - | - | $\pm 1$ | $\mu \mathrm{~A}$ |
| Ioz | Off-State Current (Hi-Z) | OV $\leq$ VouT $\leq$ Vcc | - | - | $\pm 1$ | $\mu \mathrm{~A}$ |
| RoN | Switch ON Resistance | Vcc $=$ Min., VIN $=$ OV, ION $=30 \mathrm{~mA}$ | 22 | 30 | 45 | $\Omega$ |
| RoN | Switch ON Resistance | VcC $=$ Min., VIN $=2.4 \mathrm{~V}$, ION $=15 \mathrm{~mA}$ | 22 | 37 | 55 | $\Omega$ |
| VP | Pass Voltage ${ }^{(2)}$ | VIN $=$ VCC $=5 \mathrm{~V}$, IOUT $=-5 \mu \mathrm{~A}$ | 3.7 | 4 | 4.2 | V |

## NOTES:

1. Typical values are at $\mathrm{Vcc}=5.0 \mathrm{~V}, \mathrm{TA}=25^{\circ} \mathrm{C}$.
2. Pass voltage is guaranteed but not production tested.

## TYPICAL ON RESISTANCE vs Vin AT Vcc = 5V



## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions ${ }^{(1)}$ | Max. | Unit |
| :--- | :--- | :--- | :---: | :---: |
| ICcQ | Quiescent Power Supply Current | Vcc $=$ Max., VIN $=$ GND or Vcc, $f=0$ | 3 | $\mu \mathrm{~A}$ |
| $\Delta \mathrm{IcC}$ | Power Supply Current per Control Input $\mathrm{HIGH}^{(2)}$ | Vcc $=$ Max., VIN $=3.4 \mathrm{~V}, \mathrm{f}=0$ | 3 | mA |
| ICCD | Dynamic Power Supply Current per MHZ ${ }^{(3)}$ | VcC $=$ Max., A and B pins open <br> Control Input Toggling at $50 \%$ Duty Cycle | 0.25 | $\mathrm{~mA} / \mathrm{MHz}$ |

## NOTES:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per TLL driven input $(\mathrm{VIN}=3.4 \mathrm{~V})$. $A$ and $B$ pins do not contribute to $\Delta \mathrm{lcc}$.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed but not production tested.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

$\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}, \mathrm{VcC}=5.0 \mathrm{~V} \pm 10 \%$
CLOAD $=50 \mathrm{pF}$, RLOAD $=500 \Omega$ unless otherwise noted.

| Symbol | Parameter | Min. ${ }^{(1)}$ | Typ. | Max. | Unit |
| :---: | :--- | :---: | :---: | :---: | :---: |
| tPLL <br> tPHL | Data Propagation Delay (2,4) <br> nA to nBx, nBx to nA | - | - | $1.25{ }^{(3)}$ | ns |
| tBX | Switch Multiplex Delay <br> SEL to nA | 1.5 | - | 6.5 | ns |
| tPZL <br> tPZH | Switch Turn-on Delay <br> SEL, TEST to nBx | 1.5 | - | 6.5 | ns |
| tPLZ <br> tPHZ | Switch Turn-off Delay ${ }^{(2)}$ <br> SEL, TEST to nBx | 1.5 | - | 5.8 |  |

## NOTES:

1. Minimums are guaranteed but not production tested.
2. This parameter is guaranteed but not production tested.
3. The time constant for the switch alone is of the order of 1.25 ns at $\mathrm{CL}=50 \mathrm{pF}$.
4. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

## ORDERING INFORMATION


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